Field effect transistor with diamond-like carbon channel

Background of the invention

The invention relates to a field effect transistor comprising a source and a drain connected by a channel controlled by a gate electrode separated from the channel by a gate insulator.

State of the art

A field effect transistor comprises a source and a drain that are connected by a channel. A gate electrode, separated from the channel by a gate insulator, enables the on or off state of the channel to be controlled. Conventionally, the source, drain and channel of field effect transistors are made from a semi-conducting material, for example silicon.

To produce a CMOS type inverter, a PMOS type transistor and a NMOS type transistor are assembled. Optimum operation of the inverter requires the saturation current in the PMOS transistor to be equal to the saturation current in the NMOS transistor. In a NMOS type transistor, the electric current flowing in the channel is an electron current, whereas in a PMOS type transistor, the electric current flowing in the channel is a hole current. The current is proportional to the mobility of the corresponding charge carriers. The mobility of electrons in silicon being greater than the mobility of holes in silicon, the dimensions of NMOS and PMOS type transistors are adapted so as to obtain equal saturation currents in the NMOS and PMOS transistors. Thus, the PMOS type transistor of a CMOS inverter, for example, has a larger channel width than the channel width of the associated NMOS type transistor. Miniaturization of the CMOS inverter is then limited by the dimensions of the PMOS transistor.

Object of the invention

It is one object of the invention to remedy these shortcomings and in particular to enable logic gates of small dimensions.

According to the invention, this object is achieved by the fact that the channel is constituted by a diamond-like carbon layer.

The channel can comprise N-type dopants to form a PMOS type transistor or P-type dopants to form a NMOS type transistor

It is a further object of the invention to provide a logic gate comprising PMOS type and NMOS type transistors according to the invention, the PMOS type and NMOS type transistors have substantially the same dimensions.

It is a further object of the invention to provide a transistor according to the invention obtained by a fabrication method successively comprising

- deposition of a diamond-like carbon layer on a substrate,
- deposition of an insulating gate layer on the diamond-like carbon layer,
- deposition, on the insulating gate layer, of at least one conducting layer and etching of the latter so as to form the gate electrode,
- deposition of an insulating material on flanks of the gate electrode to form a lateral insulator,
- etching of the gate insulating layer,
- etching of the diamond-like carbon layer so as to delineate the channel,
- deposition, on each side of the channel, of a semi-conducting material designed to form the source and of a semi-conducting material designed to form the drain.

According to a particular embodiment of the method according to the invention, etching of the diamond-like carbon layer is isotropic so as to obtain a retraction of the diamond-like carbon layer under the gate insulating layer.

According to another particular embodiment of the method according to the invention, the method comprises anisotropic etching of the semi-conducting materials in the zones of the substrate not covered by the gate electrode and the lateral insulator.

Brief description of the drawings

Other advantages and features will become more clearly apparent from the following description of particular embodiments of the invention given as non-restrictive examples only and represented in the accompanying drawings, in which:

Figures 1 to 5 illustrate a particular embodiment of a method for making a transistor according to the invention.

Figure 6 schematically represents a CMOS type inverter comprising transistors according to the invention.

Description of particular embodiments

The field effect transistor according to the invention comprises a channel formed by a diamond-like carbon layer. The channel can be doped by N-type dopants to form a PMOS type transistor or by P-type dopants to form a NMOS type transistor. For a doping of 10^{15} atoms per cubic centimeter, the diamond-like carbon has an electron mobility of $1800cm^2/Vs$ and a hole mobility of $1800cm^2/Vs$ at ambient temperature. Two transistors, respectively NMOS and PMOS type transistors having channels of equal widths, then have identical saturation currents. This enables logic gates to be constructed,

for example a CMOS inverter, comprising PMOS and NMOS type transistors having the same dimensions and a surface that is 28% smaller than the surface of a silicon-base CMOS inverter.

In a particular embodiment of a method for making the transistor, a diamond-like carbon layer 1 is deposited on a substrate 2, as represented in figure 1. The substrate can comprise an insulating thin layer on its surface, for example a layer of oxide having a high dielectric constant, for example alumina. Then a gate insulating layer 3 is deposited on the diamond-like carbon layer 1. A conducting layer 4 is then deposited on the gate insulating layer 3. As represented in figure 1, the conducting layer 4 can be formed by superposition of a first conducting layer 4a and of a second layer 4b that can be conducting or not, which layer can be used as masking layer for etching or embedding. The conducting layer 4a can be deposited by low-pressure chemical vapor deposition or by epitaxy. An etching step enables the conducting layer 4 to be laterally delineated by means of a mask (not shown) so as to form the gate electrode 5. Then deposition of an insulating material on the flanks of the gate electrode 5 enables a lateral insulator 6 of the gate electrode 5 to be formed. The lateral electrical insulator 6 can be achieved by depositing a layer having a thickness corresponding to the thickness of the conducting layer 4 around the gate electrode 5, followed by etching by means of a mask (not shown).

In figure 2 etching of the gate insulating layer 3 in the zones of the substrate 2 not covered by the gate electrode 5 and the insulator 6 is represented. This etching can be performed using chlorinated mixtures and a hot cathode type technique.

Etching of the diamond-like carbon layer 1, represented in figure 3, enables the channel 7 to be delineated laterally. To etch diamond-like carbon, the latter merely has to be oxidized. The $2C+O_2=2CO$ or the $C+O_2=CO_2$ reaction is fostered. A mixture of oxygen and argon can be used, argon acting as

carrier gas and enabling the oxygen to be diluted in order to finely adjust the etching rate. The diamond-like carbon layer 1 can be etched by anisotropic or isotropic etching, as represented in figure 3. By isotropic etching, a removal 8 of the diamond-like carbon layer 1 is obtained underneath the gate insulating layer 3, preferably creating a retraction extending up to underneath the gate electrode 5. Isotropic etching can be performed by low-energy oxygen plasma or by means of an oxygen flow directed onto the diamond-like carbon layer 1. Anisotropic etching can be performed by reactive ion etching using an oxygen plasma. The substrate 2 can be densified by oxygen plasma at the end of etching of the diamond-like carbon layer 1.

Figure 4 represents deposition, for example by epitaxy on the substrate 2 on each side of the channel 7, of a semi-conducting material 9a and 9b designed to respectively form the source and drain.

Anisotropic etching of the semi-conducting material 9a and 9b in the zones of the substrate 2 that are not covered by the gate electrode and the lateral insulator 6 enables the semi-conducting material 9a and 9b to be delineated laterally and the source 10 and drain 11 to be formed, as represented in figure 5. Etching of the semi-conducting material in particular enables a transistor of small size to be obtained. Fabrication of the transistor is completed by formation of contact elements connected to the source 10 and drain 11, by deposition of a metal 12 on the substrate 2, planarization, for example by mechanical-chemical means, and etching of the metal 12.

As an alternative, the source 10 and drain 11 can be made of different materials. In this case, it is possible for example to perform masking of the zone corresponding to the drain 11 during deposition of the semi-conducting material 9a designed to form the source 10, then to remove the mask, and then to mask the semi-conducting material 9a during deposition of the semi-conducting material 9b, and then remove this second mask. The materials 9a

and 9b can then be etched in anisotropic manner to respectively delineate the source 10 and drain 11, as previously.

The semi-conducting material 9a can for example be diamond, forming the source 10 of a NMOS or a PMOS type transistor. The semi-conducting material 9b can for example be diamond, germanium, gallium arsenide or indium antimonide to form the drain 11 of a NMOS type transistor, and diamond or germanium to form the drain 11 of a PMOS type transistor.

In figure 6, a PMOS type transistor 13 and a NMOS type transistor 14, forming a CMOS inverter, respectively comprise a source 10, a drain 11 and a gate electrode. Their gate electrodes 5 are connected to a common conductor 15. The PMOS and NMOS transistors have substantially the same dimensions, in particular their channel widths L are identical.

Claims

1. Field effect transistor comprising a source (10) and a drain (11) connected by a channel (7) controlled by a gate electrode (5) separated from the channel (7) by a gate insulator (3), transistor characterized in that the channel (7) is constituted by a diamond-like carbon layer (1).

2. Transistor according to claim 1, characterized in that the channel (7) comprises N-type dopants so as to form a PMOS type transistor (13).

3. Transistor according to claim 1, characterized in that the channel (7) comprises P-type dopants so as to form a NMOS type transistor (14).

4. CMOS logic gate, characterized in that it comprises PMOS type transistors (13) according to claim 2 and NMOS type transistors (14) according to claim 3, the PMOS and NMOS transistors having substantially the same dimensions.

5. Method for making a field effect transistor according to anyone of claims 1 to 3, characterized in that it successively comprises

- deposition of a diamond-like carbon layer (1) on a substrate (2),
- deposition of an insulating gate layer (3) on the diamond-like carbon layer (1),
- deposition, on the insulating gate layer (3), of at least one conducting layer (4) and etching of the latter so as to form the gate electrode (5),
- deposition of an insulating material on flanks of the gate electrode (5) to form a lateral insulator (6),
- etching of the gate insulating layer (3),
- etching of the diamond-like carbon layer (1) so as to delineate the channel (7),

- deposition, on each side of the channel (7), of a semi-conducting material (9a) designed to form the source (10) and of a semi-conducting material (9b) designed to form the drain (11).

6. Method according to claim 5, characterized in that etching of the diamond-like carbon layer (1) is isotropic so as to obtain a retraction of the diamond-like carbon layer (1) under the gate insulating layer (3).

7. Method according to claim 6, characterized in that it comprises anisotropic etching of the semi-conducting materials (9a, 9b) in the zones of the substrate (2) not covered by the gate electrode (5) and the lateral insulator (6).

Abstract

Method for making a field effect transistor with diamond-like carbon channel and resulting transistor

The field effect transistor comprises, on a substrate (2), a source (10) and a drain (11) connected by a channel (7) controlled by a gate electrode (5) separated from the channel (7) by a gate insulator (3). The channel (7) is formed by a diamond-like carbon layer. The channel (7) can comprise N-type or P-type dopants so as to respectively form a PMOS or a NMOS type transistor (13) having substantially the same dimensions, enabling logic gates to be constructed, for example a small dimension CMOS inverter. The channel (7) can be delineated by isotropic etching of the diamond-like carbon layer (1) so as to obtain a retraction of the diamond-like carbon layer (1) under the gate insulating layer (3). The source (10) and the drain (11) are delineated by anisotropic etching of a semi-conducting material in the zones of the substrate 2 that are not covered by the gate electrode (5).

(Figure 5)